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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

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Protection circuit for an integrated circuit device

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DESCRIPTION

Protection circuit for an integrated circuit device

The invention relates to an integrated circuit for protecting a circuit device from damage resulting from electrostatic discharge.

Integrated circuits, especially sensitive circuits in complementary metal oxide semiconductor (CMOS) technology, have to be protected against defects caused by a sudden electrostatic discharge (ESD). An ESD can have the consequence of a voltage breaking through a dielectric between two surfaces, in the end resulting in a short circuit, damaging the gate oxide/diffusion, the metal layers, or the contacts of the integrated circuit. The electrostatic charge existing prior to the sudden discharge of the circuit usually results from contact with an electrostatically charged object, e.g. a person or a machine.

For this purpose, i.e. protection from ESD, one or more specially designed protection circuits are usually integrated on the substrate of the circuit to be protected. Such a protection circuit is activated when a dangerous current or voltage discharge occurs and switches into a low-impedance state to keep the sensitive areas of the circuit safeguarded.

In most modern processes, the ESD protection circuits are one of several area-limiting devices, especially with regard to input/output (I/O) pads. It is thus advantageous or even necessary to reduce the chip area consumed by the protection circuit and still achieve sufficient protection. Furthermore, for high speed radio frequency (RF) I/O designs, the capacitance of the ESD protection circuit must be as low as possible, whereby the capacitance depends on the chip area used for the ESD protection.

Today, ESD protection usually relies on the breakthrough mechanism of the P-N junction of an ESD protection transistor. Curve 11 in the current voltage diagram in Fig. 1 illustrates this. The limitation in ESD robustness consists in the fact that the ESD

clamp has a differential resistance during an ESD event. The voltage drop during an ESD event reaches a value where the integrated circuit is no longer protected. Typical failures are drain damages of small N-MOS transistors or gate oxide breakdowns.

In Partovi et al. US patent 6 078 487, an electrostatic discharge protection device having a modulated control input terminal is described. The protection circuit, guarding an associated integrated circuit from damage due to electrostatic discharge, includes a N-MOS transistor serving as clamping device and a gate modulation circuit. The source and the drain of the N-MOS transistor clamp are connected between an input/output pad of the integrated circuit and a ground reference voltage. During normal operation of the integrated circuit, the gate modulation circuit disables the N-MOS transistor clamp by connecting its gate terminal to a ground reference voltage. During an ESD event, the gate modulation circuit connects the gate to the input/output pad, which enables the N-MOS transistor clamp, causing any ESD voltages and resulting currents to be shunted through the N-MOS transistor clamp to ground. However, when an ESD or electrostatic overstress (EOS) event occurs, which causes a positive voltage at the supply terminal Vdd of the clamp modulator, the voltage caused by an ESD or electrostatic overstress cannot be shunted through the N-MOS transistor clamp to ground because the N-MOS transistor clamp is disabled. Therefore, in this case an ESD or electrostatic overstress can damage the gate oxide, the metal layers or the contacts of the integrated circuit.

An object of the invention is to provide an integrated protection circuit which protects an integrated circuit having a pad, e.g. an I/O pad or a power supply pad, from electrostatic discharge or electrostatic overstress during different stress conditions.

With the integrated protection circuit according to the invention, chip area can be saved without diminishing the protection from electrostatic discharge or electrostatic overstress. Alternatively or additionally, the protection from electrostatic discharge or electrostatic overstress can be improved considerably without consuming more chip area.

The problem is solved by an integrated protection circuit with the features according to independent claim 1.

The integrated protection circuit according to the invention comprises a first transistor whose control outputs are connected between the pad and the control input of a clamping device, wherein the control outputs of the clamping device are connected between the pad and a reference voltage terminal. The protection circuit further comprises a second transistor whose control outputs are connected between the control output of the first transistor and the reference voltage terminal. Finally the protection circuit also includes a time-delay element connected between a supply voltage terminal and the control inputs of the first transistor and the second transistor.

Advantageous further developments of the invention arise from the features indicated in the dependent patent claims.

In one embodiment of the invention, the pad of the integrated protection circuit is an signal input/output pad or a power supply pad.

In another embodiment of the invention, the time-delay element of the integrated protection circuit comprises a series connection of a resistor and a capacitance.

In a further embodiment of the invention, the time-delay element of the integrated protection circuit comprises a third transistor, wherein the resistor is connected between the supply voltage terminal and the third transistor, and wherein the third transistor forms the capacitance.

Advantageously, the integrated protection circuit comprises a fourth transistor whose control outputs are connected between the reference voltage terminal and the control output of the third transistor and wherein the control input of the fourth transistor is also connected to the reference voltage terminal.

Furthermore, the first transistor of the integrated protection circuit can be a p-channel MOS transistor.

For solving the object of the invention, the second, third and fourth transistor of the integrated protection circuit can be formed as n-channel MOS transistors.

In a typical application the clamping device of the integrated protection circuit according to the invention is a n-channel MOS transistor layouted for ESD protection.

Alternatively thereto, the clamping device of the integrated protection circuit according to the invention can be a parasitic npn transistor.

Alternatively thereto, the clamping device of the integrated protection circuit according to the invention can also be formed as a thyristor.

Finally, the integrated protection circuit for protecting a circuit device can comprise a diode connected between the pad and the supply voltage terminal.

Subsequently, the invention is further explained with the drawings showing in

Fig. 1 a current voltage diagram for an ESD protection circuit according to the prior art and for an ESD protection circuit according to the invention;

Fig. 2 an embodiment of an ESD protection circuit according to the invention;

Fig. 3 an embodiment of an ESD protection circuit according to the invention used for a power pad;

Fig. 4 a block diagram of the ESD protection circuit according to the invention used for an I/O pad;

Fig. 5 a block diagram of the ESD protection circuit according to the invention used for a power pad and

Fig. 6 a block diagram with a parasitic diode in the integrated circuit.

The idea of the invention is to have a robust element which handles the ESD current during an ESD event before more sensitive internal devices can be damaged. Most common elements are diodes, N-MOS transistors and low-voltage-triggered silicone rectifiers (LVTSCR). All these devices have breakdown values higher than the operating voltage of the integrated circuitry which has to be protected.

Fig. 1 shows, beside the curve 11 illustrating the current voltage course for an ESD protection circuit according to the prior art, also a curve 12 illustrating the current voltage course for an ESD protection circuit according to the invention.

As it can be seen from this curve 12, the ESD detection circuit clamps the voltage caused by the ESD event much earlier than a conventional ESD clamp. Thereby, a lower voltage drop U1 over the clamp transistor MN4, which is shown in Fig. 2, is achieved. The voltage drop over a clamp transistor according to the prior art is indicated in Fig. 1 with U2.

The ESD test is carried out on a non operating integrated circuit (IC). During the ESD test any pulse, regardless of the voltage level, must be prevented. Therefore, it is not necessary to have an ESD protection with a trigger voltage higher than the operating voltage of the IC.

One idea of the invention is to clamp every pulse at the lowest possible voltage level. This is in common CMOS technology the threshold voltage Utr of a transistor, which is about 0.6V. During the normal operating mode of the IC this behavior is switched off and the protection circuit operates like a common voltage clamp.

In Fig. 2 an embodiment of an ESD protection circuit according to the invention is depicted. For this purpose, a supply terminal 1 for a supply voltage VDD is connected over a resistor R to the drain and gate terminals of a first n-channel metal oxide field effect transistor (N-MOSFET) MN1. The source terminal of the first N-MOS transistor NM1 is connected to the drain terminal of a second N-MOS transistor MN2. The gate terminal and the source terminal in turn are connected at the reference voltage terminal 4 to a reference potential VSS, which is the ground of the complete circuit. A p-channel MOS transistor MP1 and a third N-MOS transistor MN3 form an inverter INV whose input NET1 is connected to the source of the first N-MOS transistor NM1 and the drain terminal of the second N-MOS transistor MN2. The output NET2 of the inverter INV is connected to the gate terminal of a fourth N-MOS transistor NM4 which works as main clamp of the ESD protection circuit. The part of the ESD protection circuit inside of the doted line is called in the following active trigger control AC, while the transistor MN4 is called clamp transistor.

The protection circuit shown in Fig. 1 can be brought in two different operating modes, a normal operating mode and an event driven mode. Both modes are explained in the following.

In the first, normal, operating mode, a so-called clamp mode, the supply terminal 1 of protection circuit is powered up and the ground terminal 4 is connected to ground. In this normal operating case the circuit is not stressed with ESD or EOS. The protection circuit now operates as follows. At first, the first N-MOS transistor MN1 is turned on, this means it is conducting. Secondly, the second N-MOS transistor MN2 is turned off and gets nonconducting. Therefore, in the next step the input NET1 of the inverter INV gets high and its output NET 2 low. Finally, the main clamp MN4 is switched off. The consequence is, that the I/O pad 2 is not connected to ground but can be used as I/O pad 2.

If an overvoltage, i.e. caused by ESD or EOS, during the normal operation occurs the main clamp MN4 will act like a common used gate grounded NMOS transistor (GGNMOST) and will protect the complete circuit.

In the second mode, the event driven mode, there are four different operating conditions. In all operating conditions all nodes or pads of the circuit are floating during an ESD test except the pin to be tested and the corresponding grounded pin.

- First operating condition:

An I/O pad 2 shall be tested with a test voltage Vpad wherein the test voltage Vpad is positive versus the reference potential VSS. The circuitry works as follows. The supply voltage VDD at the supply terminal 1 is floating. Due to the capacitance formed by the gate and drain of the P-MOS transistor MP1 the transistor MP1 of the inverter INV is conducting. Therefore, the voltage at the node NET2 follows the positive test voltage Vpad at the I/O pad 2. Now, the fourth N-MOS transistor MN4 is conducting and clamps the I/O pad 2 to the reference potential VSS.

- Second operating condition:

The I/O pad 2 shall be tested with a test voltage Vpad2 wherein the test voltage Vpad2 is positive versus the supply potential VDD. Now, the supply terminal 1 is grounded and the reference potential VSS is floating.

An optional P+ diode D can forward either a bias voltage or in case of an open drain the voltage Vpad2 at the I/O pad 2 to the supply terminal 1. Otherwise the voltage Vn1 at the node NET1 is at low potential and therefore the P-MOS transistor MP1 of the inverter INV is conducting. The voltage Vn2 at the node NET2 follows the test voltage Vpad2 at the I/O pad 2, wherein the voltage Vn2 = Vpad2 - Vtr. The main clamp transistor MN4 conducts and forces the current towards the substrate. Any parasitic diode towards the supply voltage VDD will then lead the current, whereas in normal operating mode the parasitic diodes are nonconducting. A parasitic diode can be for example a n-well diode of a PMOS transistor connected between the supply potential VSS and the reference potential VDD.

- Third operating condition:

The I/O pad 2 shall be tested with a test voltage Vpad3 wherein the test voltage Vpad3 is negative versus the reference potential VSS. In the third operating condition, the voltage VSS at the supply terminal 1 is grounded and the reference potential VDD is floating.

The clamp transistor MN4 is conducting and forces the ESD current to the substrate of the integrated circuit. The parasitic N+ diode D2 leads the current towards the I/O pad 2.

Regardless of the state of the circuitry all N+/substrate diodes connected to the I/O pad 2 are driven in forward direction. Such a N+/substrate diode can be for example a N+ transistor diffusion. The ESD current flows from the reference node VSS to the I/O pad 2.

- Fourth operating condition:

The I/O pad 2 shall be tested with a test voltage Vpad4 wherein the test voltage Vpad4 is negative versus the reference potential VDD. In the fourth operating condition, the voltage VSS at the supply terminal 1 is floating and the reference potential VDD is grounded.

Either the optional diode D is forward BIASed or the transistor MP1 will conduct as described in the 1th operating condition and clamp MN4 force the ESD current to ground. Thenafter as described in 3th operating condition the current will be forced via the parasitic diodes towards VDD.

Therefore, the invention combines the robustness of the state of the art GGNMOST concept together with the advantage of an active clamping.

As shown in Fig. 3, the protection circuit can also be used for protecting the power pin or power supply pad 3 against electrostatic discharge or electrostatic overstress. For that, the power supply pad 3 is connected to the drain terminal of the P-MOS transistor MP1, the drain terminal of the fourth N-MOS transistor MN4 and the resistor R of the protection circuit. The protection circuit itself has not to be modified. Therefore it corresponds to the schema shown in Fig. 2. Regarding to the explanation of the protection circuit reference is made the above section.

Fig. 4 shows a block diagram of the ESD protection circuit according to the invention used for an I/O pad. Thereby, the active trigger circuit AC controls the clamp transistor MN4.

Fig. 5 shows a block diagram of the ESD protection circuit according to the invention used for a power pad. As already mentioned, the active trigger circuit AC controls the clamp transistor MN4.

With the help of the active clamp trigger circuit AC each kind of N-MOS transistor clamp MN4 can be driven. For example, a N-MOS transistor layouted for protection against ESD can be used as transistor clamp NM4. It is also possible to use for a big output buffer the pull down N-MOS transistor. Depending on the width to length relation this transistor can be designed as a normal N-MOS transistor or as a N-MOS transistor with special ESD constrains.

Fig. 6 shows how a parasitic diode is arranged in the integrated circuit. In normal operating mode the parasitic diode or parasitic diodes respectively are nonconducting.

In the following, an example is given for dimensioning the resistor R and the transistors MN1, MN2, MN3, MN4 and MP1. For the transistors MN1, MN2, MN3, MN4 and MP1 the dimension refers to the ratio channel width to channel length, wherein both are given in µm.

Element	Dimension	Description
R	~100 Ohm	Protects the transistor MN1;
MN1	3/0.34	Drives the node NET1 as fast as possible;
MN2	3/0.34	In close mode: The node NET1 can easily rise the potential; In open mode: Acts like the transistor MN1;
MP1	8/0.34	Drives the node NET2 as fast as possible;
MN3	1/0.34	Weak pull down; In normal mode: Pulls the node NET2 down; In event driven mode: Allows the node NET2 to drive up easy;
MN4	100/0.34	Main clamp; Layout with ESD layout properties (i.e. siprot)

Having illustrated and described a preferred embodiment for a novel protection means for an integrated circuit, it is noted that variations and modifications in the device and the method can be made without departing from the invention or the scope of the appended claims.

REFERENCE NUMBER LIST

1 power supply terminal

2 I/O pad

3 power supply pad

4 reference potential terminal

MN1 first N-MOS transistor

MN2 second N-MOS transistor

MN3 third N-MOS transistor

MN4 fourth N-MOS transistor

MP1 P-MOS transistor

NET0 node 0 or gate of MN1

NET1 first node or inverter input

NET2 second node or inverter output

INV inverter

D optional P+ diode

D2 parasitic N+ diode

VSS reference potential

VDD supply voltage

R resistor

AC active trigger circuit

U1 first voltage

U2 second voltage

CLAIMS

1. An integrated protection circuit for an integrated circuit device, comprising:
   - a first transistor (MP1) whose control outputs are connected between a pad (2, 3) and a control input of a clamping device (MN4),
   - the control outputs of said clamping device (MN4) being connected between said pad (2, 3) and a reference voltage terminal (4),
   - a second transistor (MN3) whose control outputs are connected between the control output of said first transistor (MP1) and said reference voltage terminal (4), and
   - time-delay means (R, MN1) connected between a supply voltage terminal (1) and said control inputs of said first transistor (MP1) and said second transistor (MN3).

2. The protection circuit according to claim 1, wherein
the pad (2, 3) is a signal pad (2) or a power supply pad (3).

3. The protection circuit according to claim 1 or 2, wherein
the time-delay element (R, MN1) comprises a series connection of a resistor (R) and a capacitance.

4. The protection circuit according to claim 3, wherein
the time-delay element (R, MN1) comprises a third transistor (MN1), the resistor (R) being connected between the supply voltage terminal (1) and said third transistor (MN1), said third transistor (MN1) forming the capacitance.

5. The protection circuit according to claim 4, wherein
a fourth transistor (MN2) is provided whose control outputs are connected between the reference voltage terminal (4) and the control output of the third transistor (MN1) and whose control input is connected to said reference voltage terminal (4).

6. The protection circuit according to any preceding claim, wherein
the first transistor (MP1) is a p-channel MOS transistor.

7. The protection circuit according to any preceding claim, wherein
the second, third and fourth transistor (MN1, MN2, MN3) are n-channel MOS transistors.

8. The protection circuit according to any preceding claim, wherein
the clamping device (MN4) is a n-channel MOS transistor layouted for ESD protection.

9. The protection circuit according to any of the preceding claims 1 to 7, wherein
the clamping device (MN4) is a parasitic npn transistor.

10. The protection circuit according to any of the preceding claims 1 to 7, wherein
the clamping device (MN4) is a thyristor.

11. The protection circuit according to any preceding claim, wherein
a diode (D) is connected between the pad (2) and the supply voltage terminal (1).

ABSTRACT

Protection circuit for an integrated circuit device

The integrated protection circuit according to the invention for ESD protecting an circuit device having at least one pad, e.g. a I/O pad, comprises a first transistor (MP1) whose control outputs are connected between the pad (2, 3) and the control input of a clamp transistor (MN4). The control outputs of the clamp transistor (MN4) are connected between the pad (2, 3) and a reference terminal (4). The protection circuit further comprises a second transistor (MN3) whose control outputs are connected between the control output of the first transistor (MP1) and the reference terminal (4). Finally the protection circuit also comprises time-delay elements (R, MN1) connected between a supply voltage terminal (1) and the control inputs of the first transistor (MP1) and the second transistor (MN3).

Fig. 2

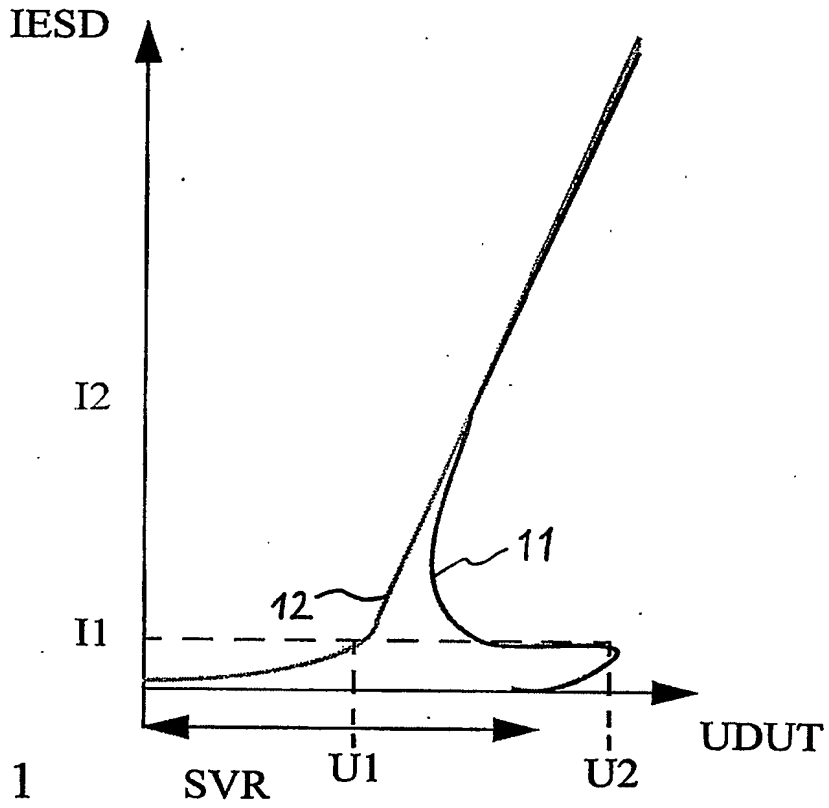
IESD
I2
I1
11
12
UDUT
SVR
U1
U2

Fig. 1

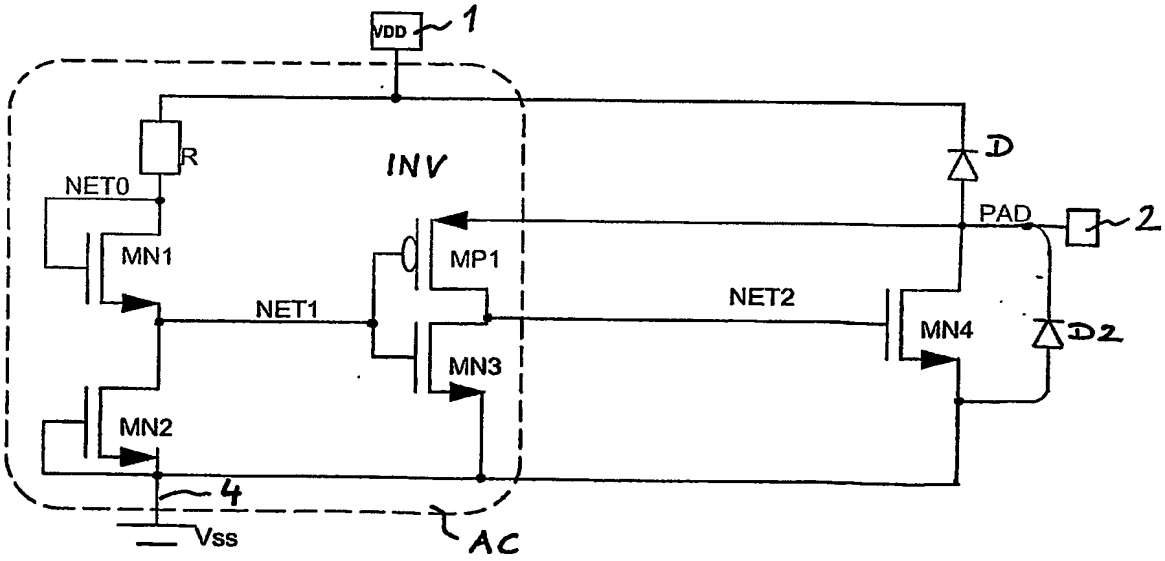
VDD
1
R
INV
D
NET0
PAD
2
MN1
MP1
NET1
NET2
MN4
D2
MN3
MN2
4
Vss
AC

Fig. 2

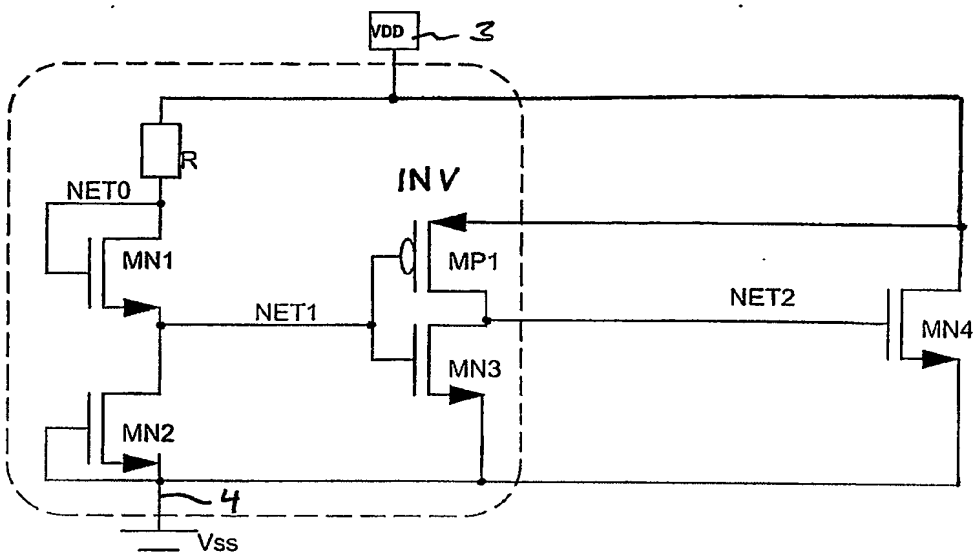

Fig. 3

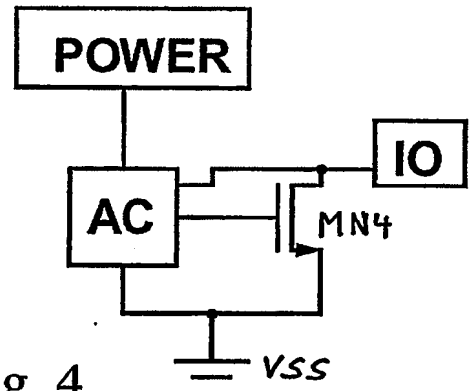

Fig. 4

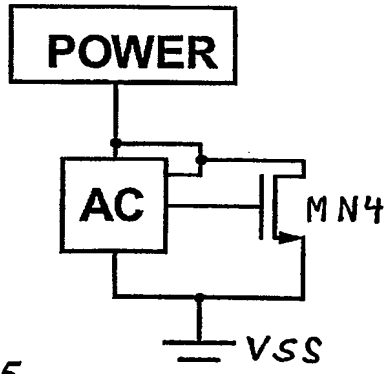

Fig. 5

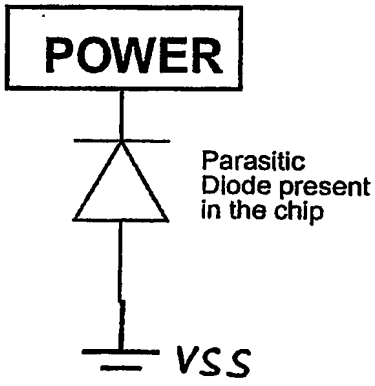

Fig. 6

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